wherein more than one memory segment (X,Y,Z;A,B,C,D,E) of the memory device (S) is required for storing an insertion picture (Kj), and in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) are cyclically overwritten by the insertion pictures (Kj) in a predetermined order.

15. The method of claim 14 wherein the memory segments (X,Y,Z;A,B,C,D,E) are the same size.

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16. The method of claim 14 wherein in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area (I,II; I,II,III) holding the currently written insertion picture, a decision is made as to whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out.

17. The method of claim 14 wherein the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

18. The method of claim 17 wherein the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

19. The method of claim 18 wherein a memory segment has a storage capacity of 1/VD times the storage capacity required for an insertion picture and the decision criterion that is applied is whether the last memory segment (II; III) required for the currently written insertion picture is already being written too.

20. The method of claim 14 wherein the insertion pictures (Kj) and main pictures (Hi) are fields of a monitor picture.

21. The method of claim 14 wherein a comparison is made to determine whether a main picture (Hi) and an insertion picture (Ki) to be inserted into the latter have an identical field position, and, in the case of a differing field position, an identical field position is achieved by address shifting of the main picture (Hi) or of the insertion picture.

22. A circuit arrangement for picture-in-picture insertion having a memory device (S) for storing vertically decimated insertion pictures (Kj=K1, K2,...), the memory device (S) having a storage capacity of less than two insertion pictures (Kj) and being subdivided into memory segments (X,Y,Z;A,B,C,D,E) which can be continuously overwritten by the insertion pictures (Kj), having a control device (3) for reading out the vertically decimated insertion pictures from the memory device (S) and for inserting the insertion pictures (Kj) read out into a sequence of main pictures (Hi=H1, H2...), and
having a decision device for deciding whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out,

wherein each memory segment (X,Y,Z;A,B,C,D,E) has a storage capacity of less than one insertion picture (Kj), and
in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) can be cyclically overwritten by the insertion pictures (Kj) in a predetermined order.

23. The circuit arrangement of claim 22 wherein the memory segments (X,Y,Z;A,B,C,D,E) are the same size.

24. The circuit arrangement of claim 22 wherein the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

25. The circuit arrangement of claim 24 wherein the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).